SONY

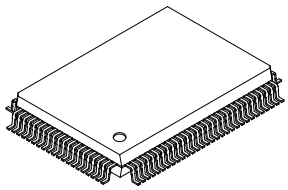
CXD2428Q

Video Scan Converter

Description

The CXD2428Q is an IC which generates control signals and performs line interpolation calculations for field memory (CXK1206AM/ATM) in order to perform video signal scanning line conversion. In addition, this IC performs the aspect conversion of the ZOOM mode and WIDE-ZOOM mode in order to support wide screens.

100 pin QFP (Plastic)



Features

- Video signal (NTSC/PAL) scanning line conversion function
- ZOOM function
  (Function to cut top and bottom areas of 4:3 image and expand it to 16:9)
- WIDE-ZOOM function
  (Function to vertically compress 4:3 image and expand it to 16:9)
- Operating frequency: 28.6MHz (typ.)

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Operating Conditions

Supply voltage	V_{DD}	4.5 to 5.5	V

Applications

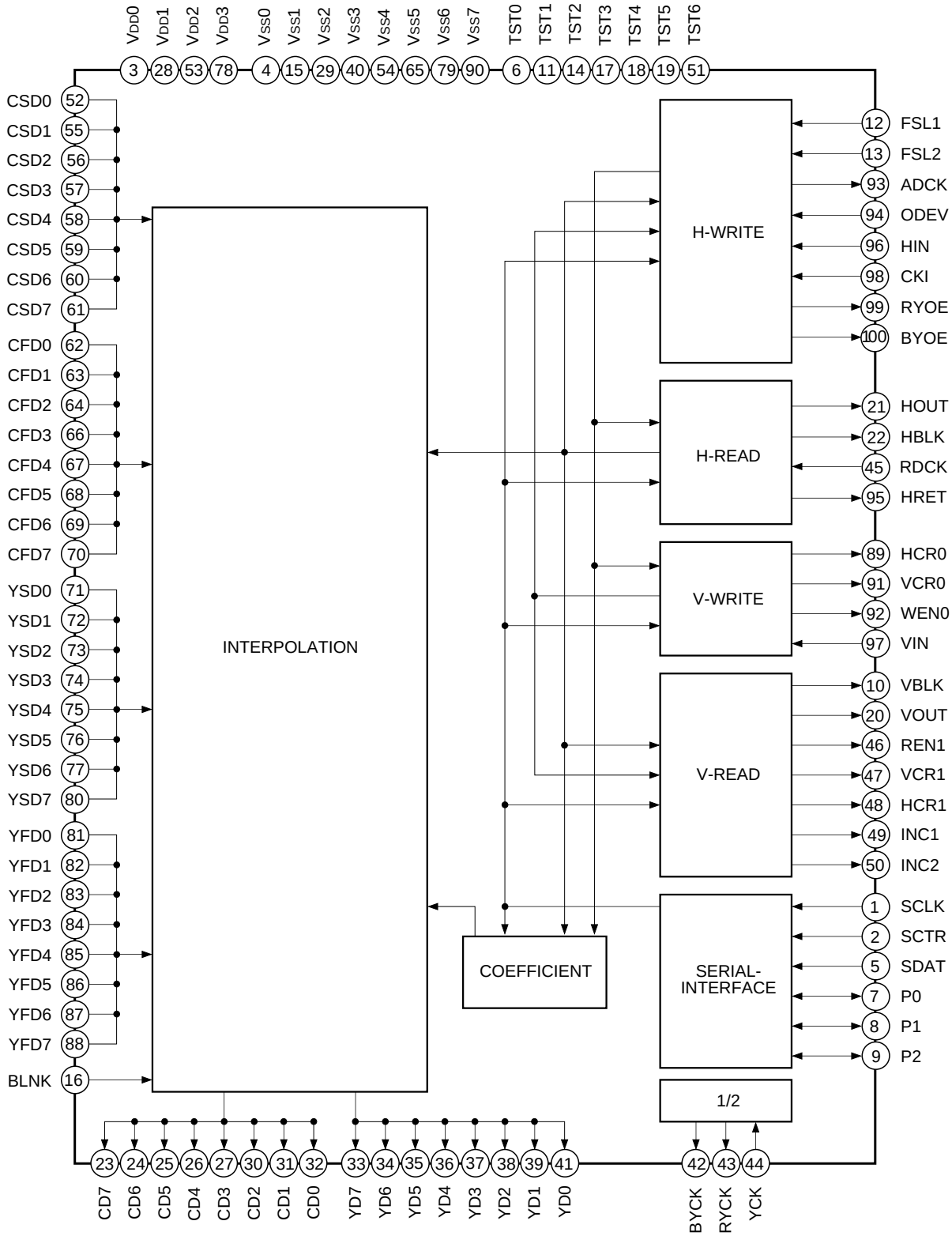
Liquid crystal projectors, etc.

Structure

Silicon gate CMOS IC

E95442-ST

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	SCLK	I	Serial transfer clock
2	SCTR	I	Serial transfer control
3	$V_{DD}0$	—	Power supply
4	$V_{SS}0$	—	GND
5	SDAT	I	Serial transfer data
6	TST0	O	Leave open.
7	P0	I/O	I/O port
8	P1	I/O	I/O port
9	P2	I/O	I/O port
10	VBLK	O	Vertical blanking output
11	TST1	I	Fixed to high.
12	FSL1	I	Field identification selection (High: internal, Low: external)
13	FSL2	I	Field information polarity switching
14	TST2	I	Fixed to low.
15	$V_{SS}1$	—	GND
16	BLNK	I	Output data control (High: black display)
17	TST3	I	Fixed to high.
18	TST4	I	Leave open.
19	TST5	I	Leave open.
20	VOUT	O	Vertical sync signal output
21	HOUT	O	Horizontal sync signal output
22	HBLK	O	Horizontal blanking signal
23	CD7	O	B-Y/R-Y data output (MSB)
24	CD6	O	B-Y/R-Y data output
25	CD5	O	B-Y/R-Y data output
26	CD4	O	B-Y/R-Y data output
27	CD3	O	B-Y/R-Y data output
28	$V_{DD}1$	—	Power supply
29	$V_{SS}2$	—	GND
30	CD2	O	B-Y/R-Y data output
31	CD1	O	B-Y/R-Y data output
32	CD0	O	B-Y/R-Y data output (LSB)
33	YD7	O	Y data output (MSB)
34	YD6	O	Y data output
35	YD5	O	Y data output
36	YD4	O	Y data output
37	YD3	O	Y data output

Pin No.	Symbol	I/O	Description
38	YD2	O	Y data output
39	YD1	O	Y data output
40	$V_{SS}3$	—	GND
41	YD0	O	Y data output (LSB)
42	BYCK	O	DA converter (B-Y) clock output
43	RYCK	O	DA converter (R-Y) clock output
44	YCK	I	DA converter clock input
45	RDCK	I	Readout clock input
46	REN1	O	Readout memory enable
47	VCR1	O	Readout memory vertical clear
48	HCR1	O	Readout memory horizontal clear
49	INC1	O	Readout memory line increment
50	INC2	O	Readout memory line increment
51	TST6	I	Fixed to high.
52	CSD0	I	B-Y/R-Y lower line data input (LSB)
53	$V_{DD}2$	—	Power supply
54	$V_{SS}4$	—	GND
55	CSD1	I	B-Y/R-Y lower line data input
56	CSD2	I	B-Y/R-Y lower line data input
57	CSD3	I	B-Y/R-Y lower line data input
58	CSD4	I	B-Y/R-Y lower line data input
59	CSD5	I	B-Y/R-Y lower line data input
60	CSD6	I	B-Y/R-Y lower line data input
61	CSD7	I	B-Y/R-Y lower line data input (MSB)
62	CFD0	I	B-Y/R-Y upper line data input (LSB)
63	CFD1	I	B-Y/R-Y upper line data input
64	CFD2	I	B-Y/R-Y upper line data input
65	$V_{SS}5$	—	GND
66	CFD3	I	B-Y/R-Y upper line data input
67	CFD4	I	B-Y/R-Y upper line data input
68	CFD5	I	B-Y/R-Y upper line data input
69	CFD6	I	B-Y/R-Y upper line data input
70	CFD7	I	B-Y/R-Y upper line data input (MSB)
71	YSD0	I	Y lower line data input (LSB)
72	YSD1	I	Y lower line data input
73	YSD2	I	Y lower line data input
74	YSD3	I	Y lower line data input

Pin No.	Symbol	I/O	Description
75	YSD4	I	Y lower line data input
76	YSD5	I	Y lower line data input
77	YSD6	I	Y lower line data input
78	$V_{DD}3$	—	Power supply
79	$V_{SS}6$	—	GND
80	YSD7	I	Y lower line data input (MSB)
81	YFD0	I	Y upper line data input (LSB)
82	YFD1	I	Y upper line data input
83	YFD2	I	Y upper line data input
84	YFD3	I	Y upper line data input
85	YFD4	I	Y upper line data input
86	YFD5	I	Y upper line data input
87	YFD6	I	Y upper line data input
88	YFD7	I	Y upper line data input (MSB)
89	HCR0	O	Write memory horizontal clear
90	$V_{SS}7$	—	GND
91	VCR0	O	Write memory vertical clear
92	WEN0	O	Write memory enable
93	ADCK	O	AD converter clock
94	ODEV	I	Field information input
95	HRET	O	Phase comparison output
96	HIN	I	Horizontal sync signal input
97	VIN	I	Vertical sync signal input
98	CKI	I	Write clock input
99	RYOE	O	AD converter (R-Y) enable
100	BYOE	O	AD converter (B-Y) enable

Electrical Characteristics

DC Characteristic

(V_{DD} = 5.0V ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pin
Input, output voltage	V_I, V_O		Vss		V_{DD}	V	
Input voltage 1	V_{IH}		0.7V_{DD}			V	*1
	V_{IL}				0.3V_{DD}		
Input voltage 2	V_{IH}		0.8V_{DD}			V	*2
	V_{IL}				0.2V_{DD}		
Output voltage 1	V_{OH1}	I_{OH} = –2mA	V_{DD} – 0.8			V	*3
		I_{OL} = 4mA			0.4		
Output voltage 2	V_{OH1}	I_{OH} = –4mA	V_{DD} – 0.8			V	*4
		I_{OL} = 8mA			0.4		
Output voltage 3	V_{OH1}	I_{OH} = –6mA	V_{DD} – 0.8			V	*5
		I_{OL} = 12mA			0.4	µA	
Input leak current	I_{LI1}	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*6
	I_{LI2}	V_{IN} = V_{SS}	–40	–100	–240	µA	*7
	I_{LI3}	V_{IN} = V_{DD}	40	100	240	µA	*8
	I_{LI4}	V_{IN} = V_{SS} or V_{DD}	–40		40	µA	*9
Output leak current	I_{LZ}	V_{IN} = V_{SS} or V_{DD}	–40		40	µA	*10
Current consumption	I_{DD}	V_{DD} = 5.0V		70		mA	

*1 All input pins other than *2

*2 Pins 1, 2, 5, 96 and 97

*3 All output pins other than *4 and *5

*4 Pins 10, 22, 42, 43, 46 to 50, 89, 91, 92 and 93

*5 Pins 20 and 21

*6 All input pins other than *7, *8 and *9

*7 Pins 11, 12, 19 and 51

*8 Pins 13, 14, 16, 17 and 18

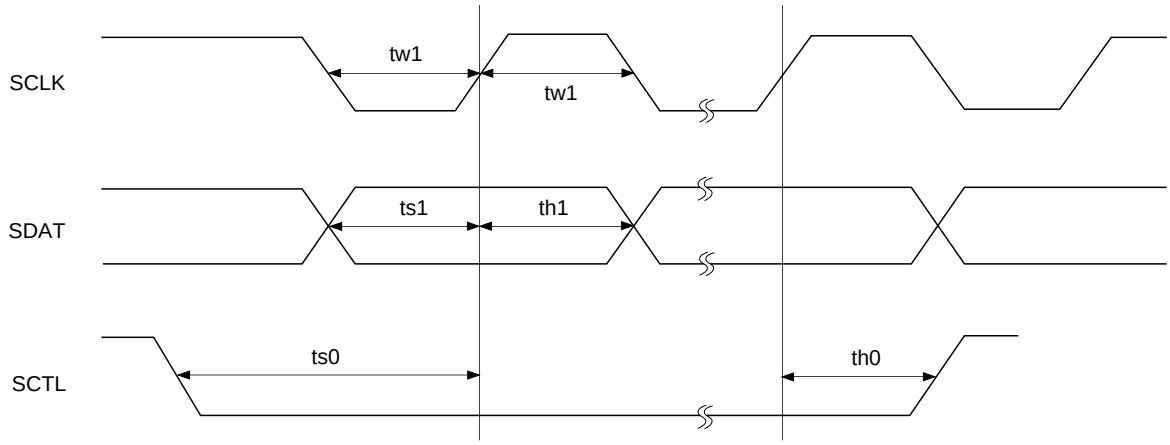
*9 Pins 7, 8 and 9

*10 Pin 6

I/O Pin Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
Input/output pin capacitance	$C_{I/O}$			11	pF

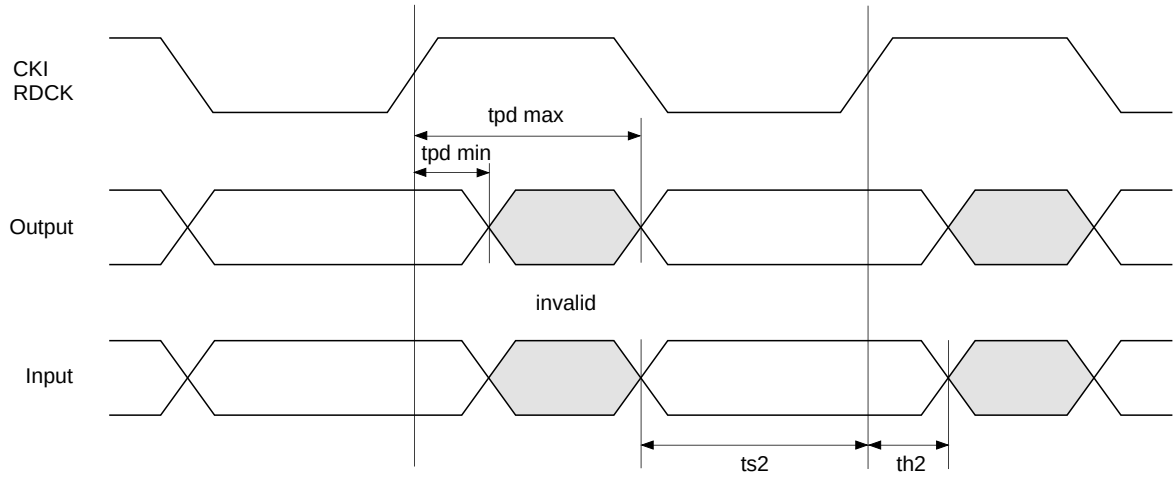
Serial Block AC Characteristics



(V_{DD} = 5.0V ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Symbol	Item	Min.	Max.
ts1	Setup time of SDAT in relation to the rise of SCLK	100ns	
th1	Hold time of SDAT in relation to the rise of SCLK	100ns	
tw1	SCLK pulse width	100ns	
ts0	Setup time of SCTL in relation to the rise of SCLK	100ns	2tw1
th0	Hold time of SCTL in relation to the rise of SCLK	100ns	2tw1

AC Characteristics



1) Output block (V_{DD} = 5.0V ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	tpd min	tpd max	Condition
Delay of ADCK in relation to CKI	3ns	28ns	Load 25pF
Delay of HCR0, VCR0 and WEN0 in relation to CKI	10ns	70ns	
Delay of REN1, VCR1, HCR1, INC1 and INC2 in relation to RDCK	6ns	32ns	
Delay of HOUT in relation to RDCK	5ns	30ns	Load 20pF
Delay of VOUT in relation to RDCK	7ns	45ns	
Delay of RYCK and BYCK in relation to YCK	1ns	22ns	
Delay of YD0 to YD7 and CD0 to CD7 in relation to RDCK	5ns	38ns	
Delay of HRET in relation to CKI	5ns	32ns	
Delay of BYOE and RYOE in relation to CKI	2ns	25ns	

2) Input block

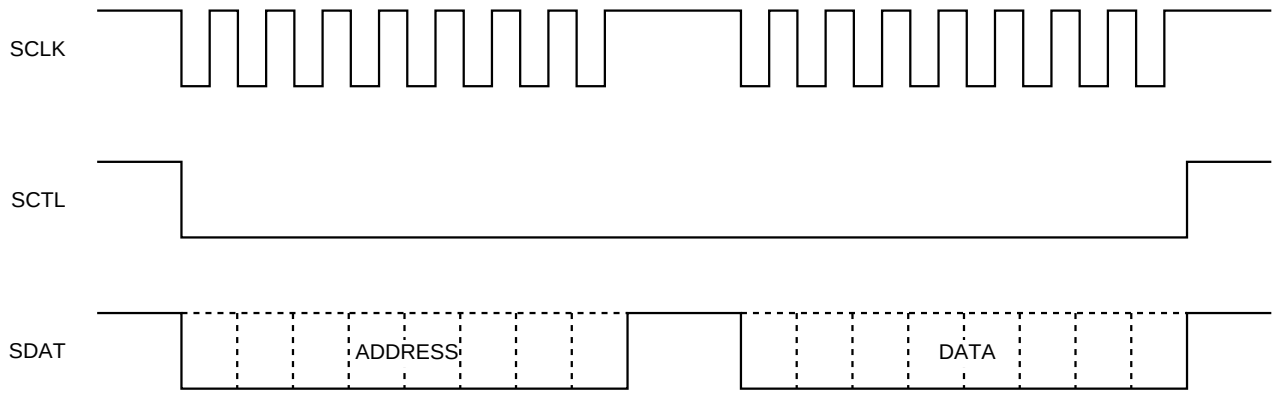
Item	ts2	th2
Setup and hold time of CSD0 to CSD7, CFD0 to CFD7, YSD0 to YSD7 and YFD0 to YFD7 in relation to RDCK	9ns	3ns
Setup and hold time of HIN in relation to CKI	3ns	3ns
Setup and hold time of VIN in relation to CKI	0ns	20ns
Setup and hold time of YCK in relation to CKI	20ns	2ns

Description of Operation

1. CXD2428Q Control System

The operation timing of this IC is controlled by serial data.

An 8-bit address and 8-bit data are sequentially transferred from the falling edge of SCTL, and each control data is taken in at the rising edge of SCLK up to the rising edge of SCTL.



Serial transfer timing

2. Control Mode

The following timing and modes are changed by control data:

Variable	Address	Function
H SHIFT	00H	Horizontal write start timing
V SHIFT	10H	Vertical write start timing
H PHASE	20H	Horizontal readout start timing
V PHASE	30H	Vertical readout start timing
H SZ RD	40H	Number of readout line dots (0 to 7 bits)
	50H	Number of readout line dots (8 to 10 bits)
H SZ WR	41H	Number of write line dots (0 to 7 bits)
	51H	Number of write line dots (8 to 10 bits)
LN DAT0 to 7	60 to 67H	Conversion mode address
MD DAT0 to 7	70 to 77H	Conversion mode data
TOP BLK	A0H	Vertical blanking rise timing
BTM BLK	B0H	Vertical blanking fall timing
LFT BLK	C0H	Horizontal blanking rise timing
RGT BLK	D0H	Horizontal blanking fall timing
IODAT	80H	I/O port output data∗1
IOSL	E0H	OUT port select∗2
TEST	90H	∗3

∗1 Transfer xxxx.1xxx (binary) for PAL (4:3 display) and xxxx.0xxx (binary) for the other systems.

∗2 Transfer 00 (hexadecimal).

∗3 Transfer 00 (hexadecimal).

3. Scanning Line Conversion Function

LN DAT (address 6x) and MD DAT (address 7x) are data which indicate scanning line conversion coefficients.

There are the following 8 conversion coefficients:

1.67/1.75/2/2.22/2.33/2.67/2.8 = K

$$K = \frac{\text{number of scanning lines of output signal}}{\text{number of scanning lines of input signal}}$$

The conversion coefficient equals the ratio of one scanning line to scan lines generated by interpolation. The coefficient can be changed on the screen.

In the WIDE-ZOOM mode, compression and expansion on the screen can be changed by combining these 8 coefficients as desired.

Compression and expansion are carried out by setting the coefficient and the number of switching lines.

The upper 6 MD DAT bits (bits 3 to 8) provide coefficient data.

The lower 2 MD DAT bits (bits 1 and 2) and 8 LN DAT bits provide line number data.

The coefficients and corresponding MD DAT are shown below.

Coefficient	MD DAT MSB LSB
1.67	000100xx
1.75	001000xx
2.0	000001xx 000000xx *
2.1	010000xx
2.22	011100xx
2.33	101000xx
2.67	110000xx
2.8	110110xx

* The interpolation coefficient 2.0 has two modes which are determined by the value of bit 3.
  When bit 3 is 1, an interpolation line is generated by outputting the same signal as that of the preceding line. This mode realizes images with a higher vertical resolution.
  When bit 3 is 0, an interpolation line is output by averaging signals of the preceding and following lines. This mode realizes images with smoother diagonal lines.

4. DA Converter Clock

RYCK and BYCK, which are YCK halved and phase inverted, are output as D/A converter clocks.

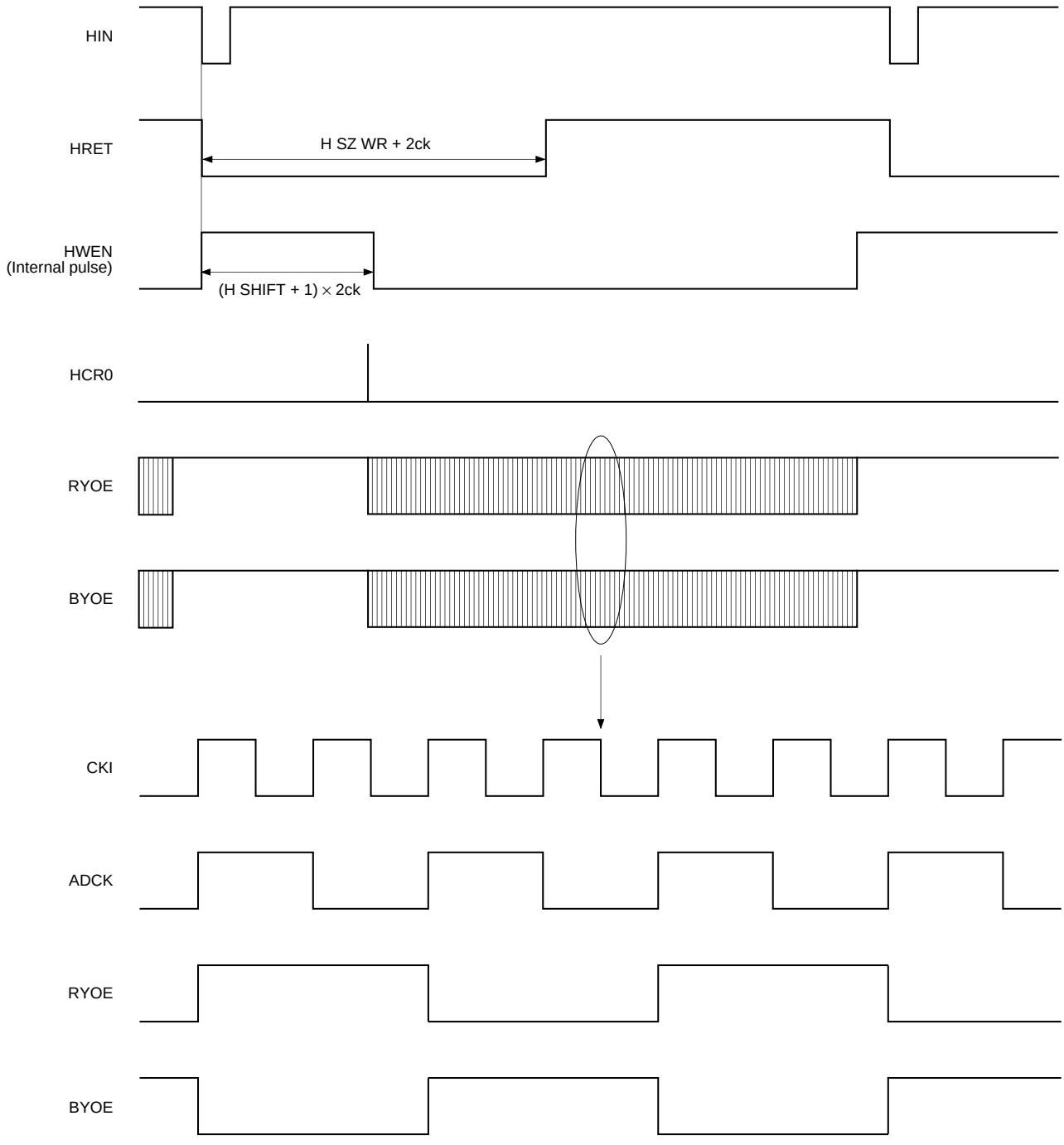
5. Output Control

A black signal is output when BLNK is high.

Mode Setting and Operation

1. Horizontal Write

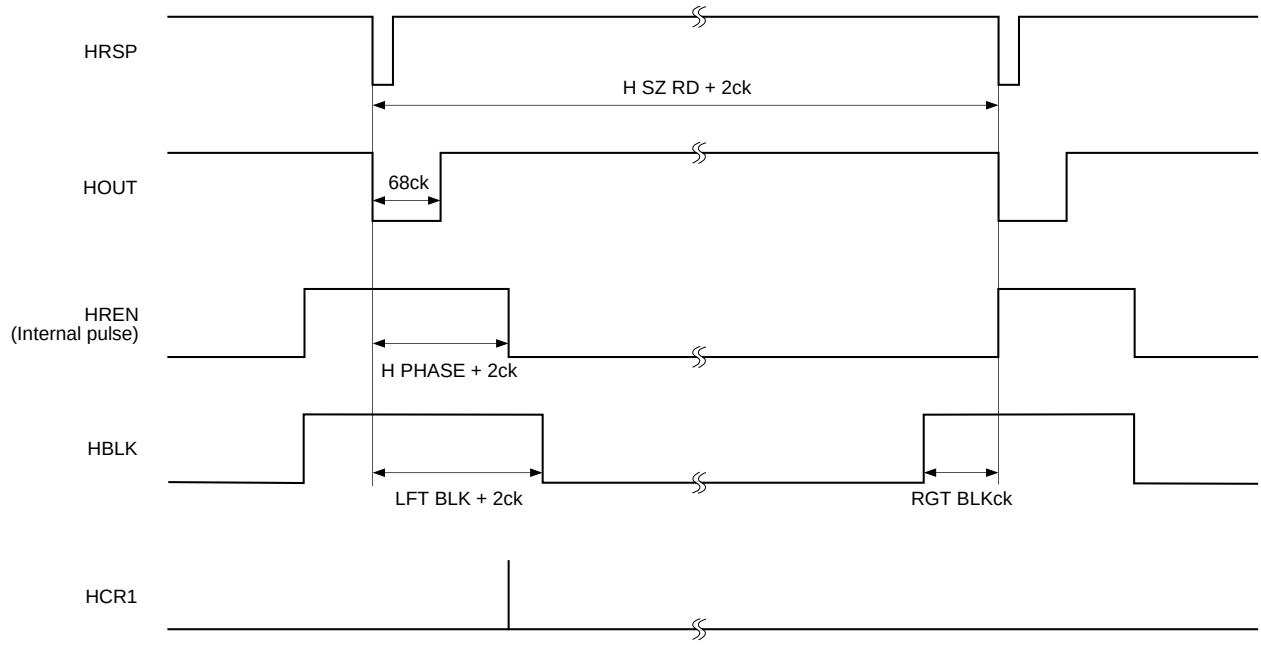
CKI is input after phase comparison with HSYNC input.
PLL frequency division value is set by H SZ WR (standard 38C (hexadecimal)), and HRET is output.
Write start timing is set by H SHIFT.
An ADCK pulse, which is CKI halved, is output.
The enable pulses RYOE and BYOE for R-Y and B-Y A/D converter are output.



2. Horizontal Readout

In this IC, the readout and write clocks are asynchronous.
The readout 1H sample coefficient is set by H SZ RD.

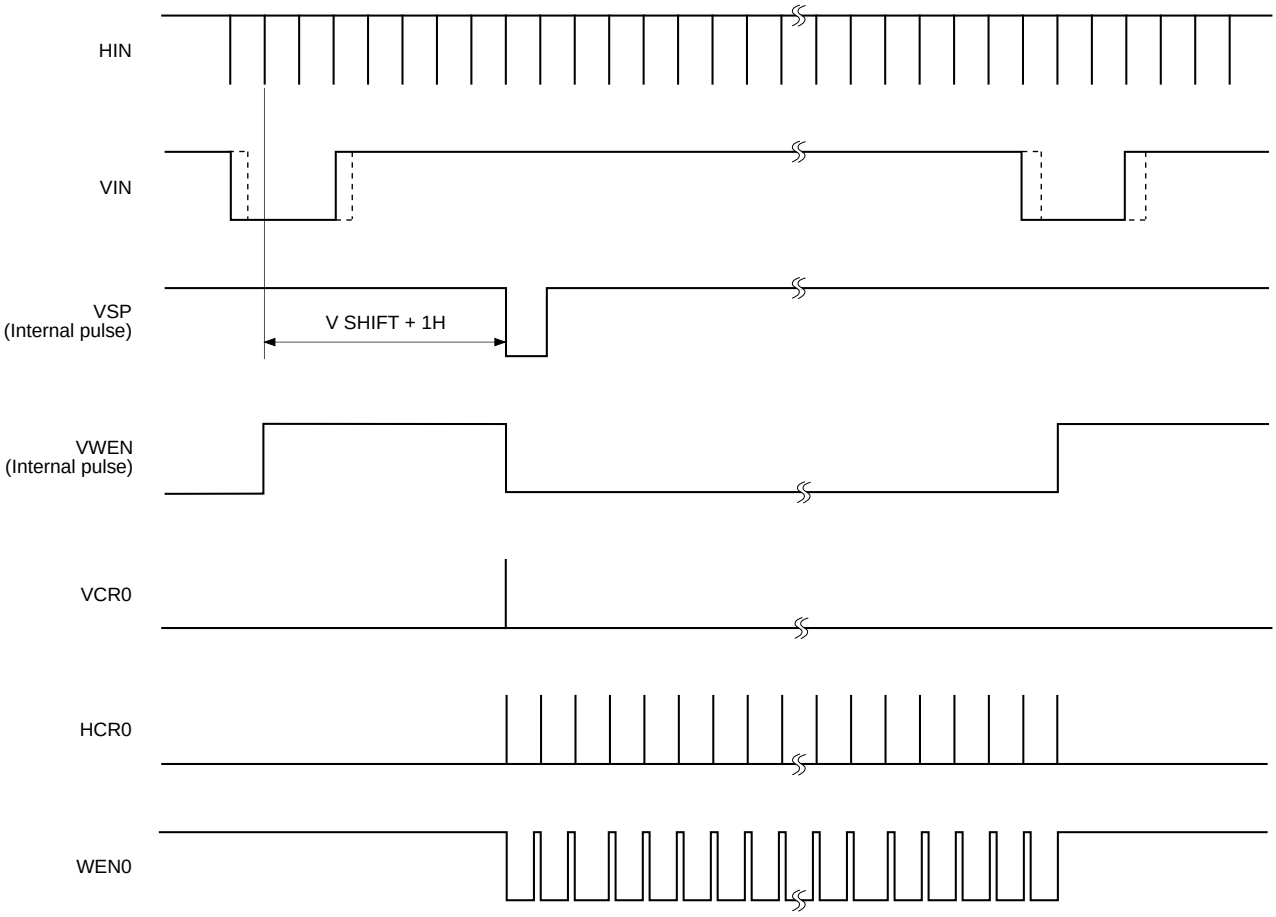
An HOUT pulse with a pulse width of 68ck is output from horizontal readout reference pulse HRSP (internal pulse).
Readout start timing is set by H PHASE.
The HBLK pulse set by LFT BLK and RGT BLK is output. However, this pulse does not stop readout, so it has no relation to the actual blanking interval.



3. Vertical Write

Write start timing is set by V SHIFT.

The CXK1206AM/ATM write control pulses VCR0, HCR0 and WEN0 are output.



4. Vertical Readout

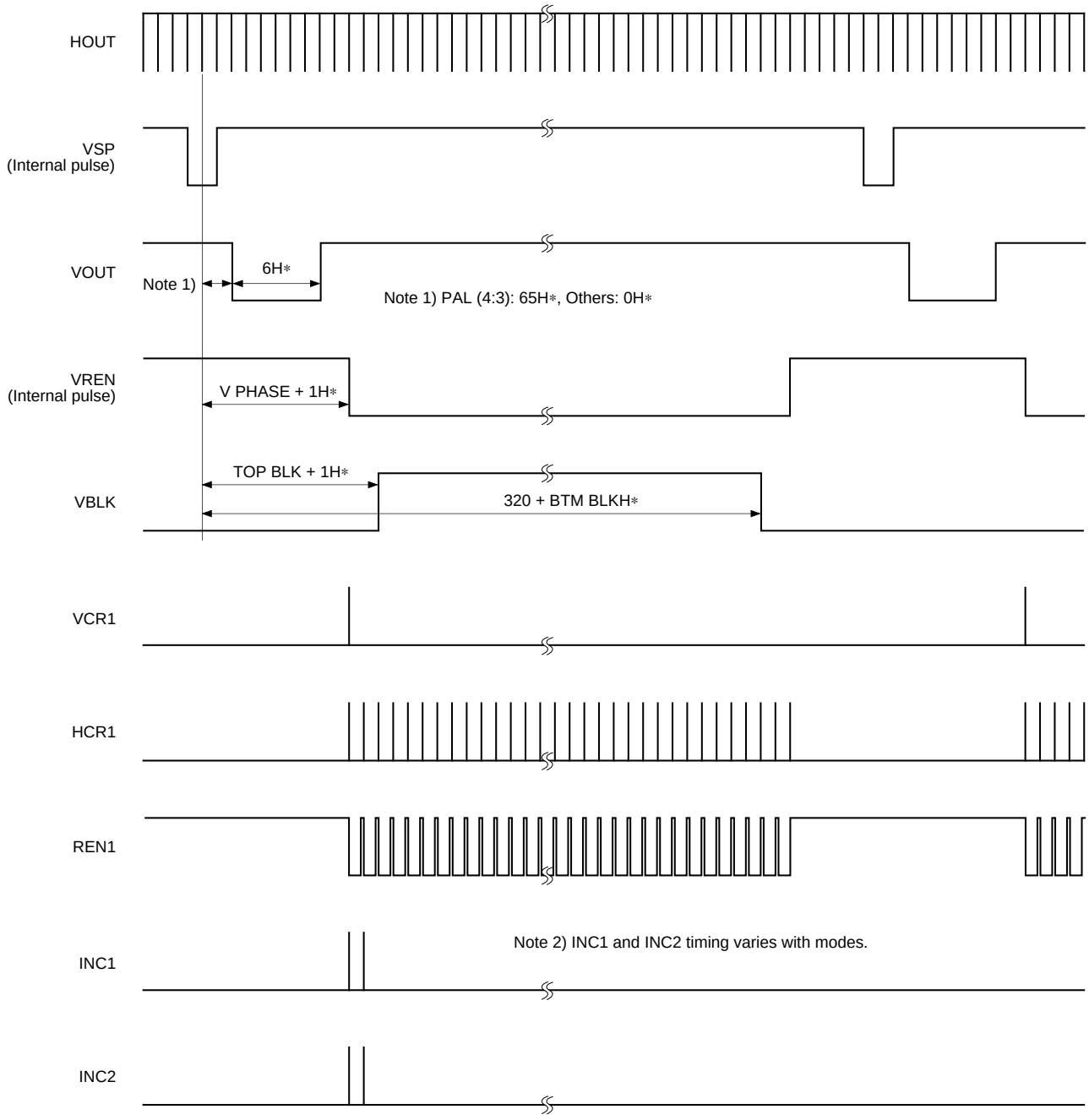
The VBLK pulse set by TOP BLK and BTM BLK is output. However, this pulse does not stop readout, so it has no relation to the actual blanking interval.

Readout start timing is set by V PHASE.

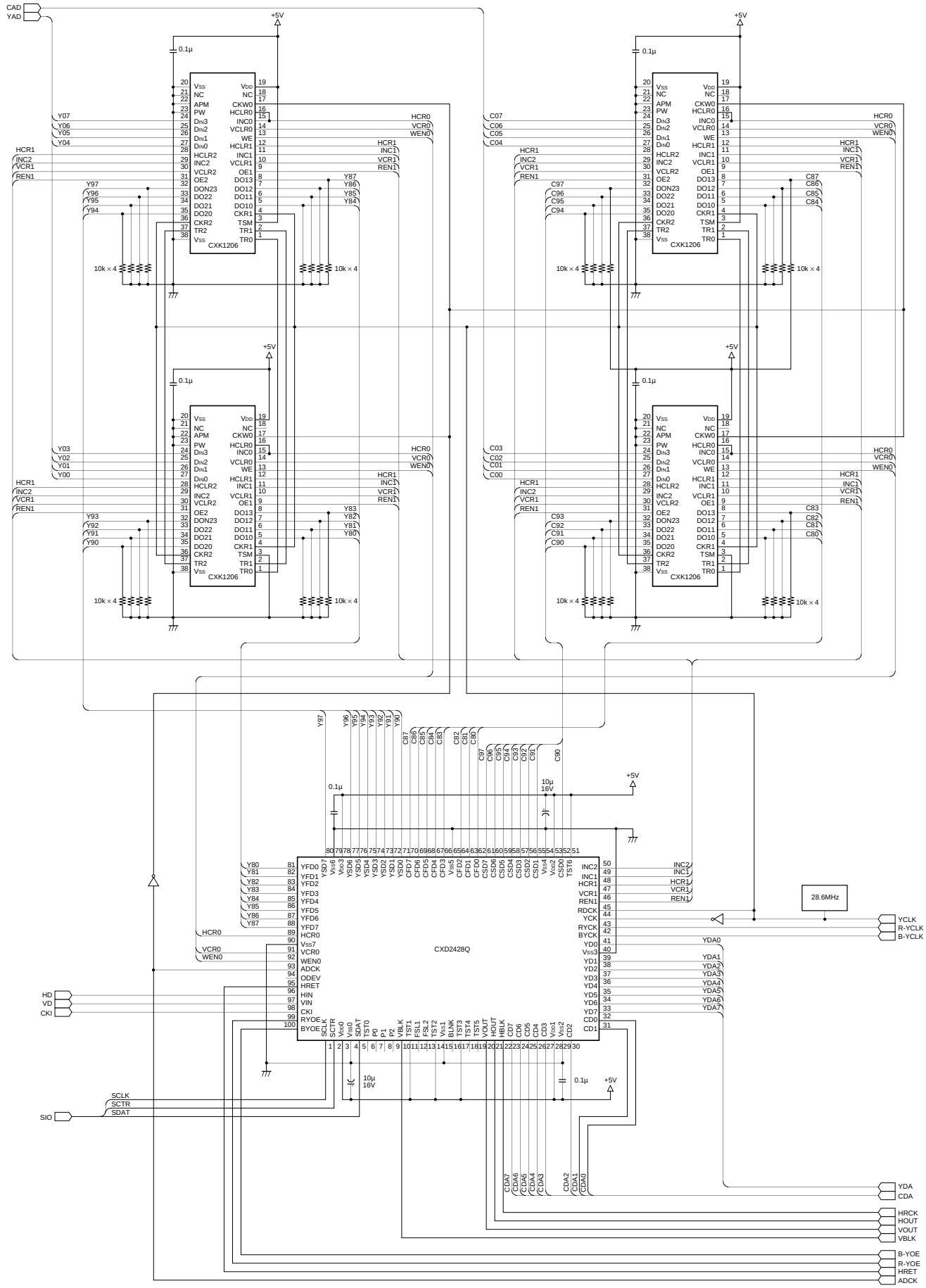
The CXK1206AM/ATM readout control pulses VCR1, HCR1, REN1, INC1 and INC2 are output.

The VSP pulse (internal pulse) corresponding to V SHIFT is the vertical readout reference pulse.

A VOUT pulse with a pulse width of 6H∗ (∗ indicates double scan H) is output.



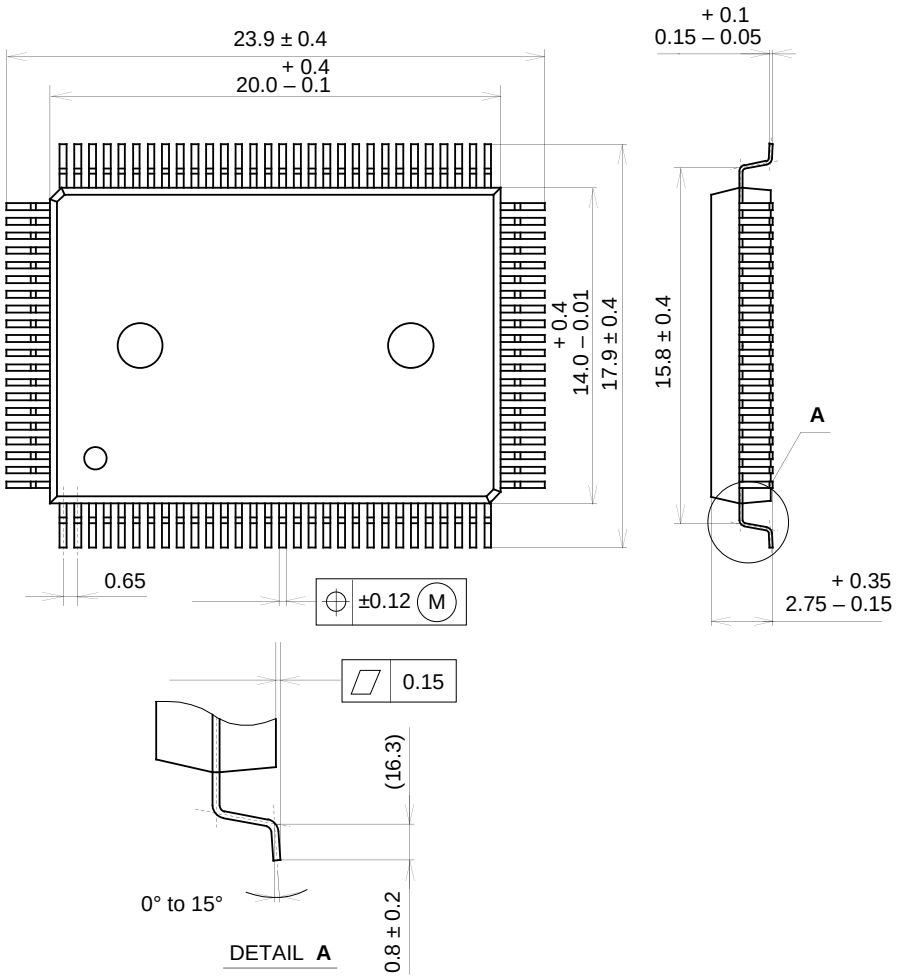
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g